architectural register are prescribed by a macro instruction. The bypass logic is coupled to the translator. The bypass logic routes the micro instruction to the execution logic. The bypass logic includes a mode detector and native instruction routing logic. The mode detector detects the native bypass macro instruction, and directs that the translator cease instruction translation. The native instruction routing logic is coupled to the mode detector. The native instruction routing logic receives the micro instruction from the macro instruction bus, and provides the micro instruction to the micro instruction bus, thereby circumventing the translator.

In a further aspect, it is a feature of the present invention to provide a microprocessor for executing micro instructions directly from memory. The microprocessor includes translation logic, mode detection logic, and an instruction router. The translation logic receives macro instructions from the memory, and decodes the macro instructions into corresponding micro instructions for execution by the microprocessor. The mode detection logic is coupled to the translation logic. The mode detection logic detects bypass macro instructions, and directs the microprocessor to execute the micro instructions directly from the memory rather than via the translation logic. The bypass macro instructions include a native branch macro instruction and a native branch return macro instruction. The native branch macro instruction directs that program control be transferred to a target address, where the translation logic decodes the native branch macro instruction into an unconditional jump native instruction directing that program control be transferred to the target address, and where the target address contains the micro instructions, and where the target address is explicitly prescribed by contents of an architectural register. The contents and the architectural register are prescribed by a macro instruction. The native branch return macro instruction directs that program control be transferred to a return address. The instruction router is coupled to the mode detection logic. The instruction router receives the micro instructions, and routes the micro instructions to execution logic, thereby bypassing the translation logic.

~~To address the above detailed deficiencies, it is an object of the present invention to provide a branch prediction apparatus that provides accurate branch predictions by~~